**WHAT IS CLAIMED IS:**

1. A static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells, each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program.

2. The SRAM device as set forth in Claim 1 wherein said biasing circuit initially applies power only to said first inverter.

3. The SRAM device as set forth in Claim 2 wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state.

4. The SRAM device as set forth in Claim 3 wherein said biasing circuit subsequently applies power to said second inverter.

5. The SRAM device as set forth in Claim 4 wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state.

6. The SRAM device as set forth in Claim 1 wherein said biasing circuit initially applies power only to said second inverter.

7. The SRAM device as set forth in Claim 6 wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state.

8. The SRAM device as set forth in Claim 7 wherein said biasing circuit subsequently applies power to said first inverter.

9. The SRAM device as set forth in Claim 8 wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state.

10. The SRAM device as set forth in Claim 1 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

11. A data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU, said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing bits of said boot-up program, each of said storage cells comprising:

a data latch having an input and an output, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device.

12. The data processor as set forth in Claim 11 wherein said biasing circuit initially applies power only to said first inverter.

13. The data processor as set forth in Claim 12 wherein said initial application of power only to said first inverter forces said first inverter output to a Logic 1 state.

14. The data processor as set forth in Claim 13 wherein said biasing circuit subsequently applies power to said second inverter.

15. The data processor as set forth in Claim 14 wherein said subsequent application of power to said second inverter forces said second inverter output to a Logic 0 state.

16. The data processor as set forth in Claim 11 wherein said biasing circuit initially applies power only to said second inverter.

17. The data processor as set forth in Claim 16 wherein said initial application of power only to said second inverter forces said second inverter output to a Logic 1 state.

18. The data processor as set forth in Claim 17 wherein said biasing circuit subsequently applies power to said first inverter.

19. The data processor as set forth in Claim 18 wherein said subsequent application of power to said first inverter forces said first inverter output to a Logic 1 state.

20. The data processor as set forth in Claim 11 wherein said biasing circuit comprises a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

21. For use in a storage cell in a static random access memory (SRAM) device, the storage cell having an input and an output and comprising 1) a first inverter having an input coupled to the storage cell input and an output coupled to the storage cell output and 2) a second inverter having an input coupled to the storage cell output and an output coupled to the storage cell input, a method of forcing the storage cell output to a known logic state when power is applied to the SRAM device comprising the step of:

initially applying power only to one of the first inverter and the second inverter, wherein the initial application of power only to one of the first inverter and the second inverter forces a selected one of the first inverter output and the second inverter output to a Logic 1 state.

22. The method as set forth in Claim 21 including the further step of subsequently applying power to the initially unpowered one of the first inverter and the second inverter, wherein the subsequent application of power to the initially unpowered one of the first inverter and the second inverter forces the output of the unselected one of the first inverter output and the second inverter output to a Logic 0 state.